Notice of Allowability	Application No.	Applicant(s)	
	09/881,226	MAY ET AL.	
	Examiner	Art Unit	
	Zhuo H. Li	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *1/26/2006*.

2. ☒ The allowed claim(s) is/are *1-12 and 46-53*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☒ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT AND STATEMENT OF REASONS FOR ALLOWANCE

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

In the specification, page 13, line 29, --assigned patent number 6,803,785, filed on June 12, 2001, attorney docket number **015114-053400US**,--

EXAMINER'S STATEMTN OF REASONS FOR ALLOWANCE

2. Claims 1-12 and 46-53 are allowed.

3. The following is an examiner's statement of reasons for allowance:

Applicant's invention is drawn to a programmable logic integrated circuit and method for transferring data from first and second ports to a plurality of memory cells in a dual-port SRAMs controlled by the user-defined lock size defines a lockable portion and non-lockable portion of the plurality of memory cells, in order to prevent the conflicts of simultaneously accessing by both ports of some or all of the memory locations (i.e., an arbiter coupled to the first and second ports, arbitrates access to the memory by the first and second ports, and when the second port is

accessing a subset of the first plurality of memory cells, the arbiter prevents the first port from accessing the first plurality of memory cells but allows the first port to access the second plurality of memory cells, and when the second port is accessing a subset of the second plurality of memory cells, the arbiter allows the first port to access the first and second pluralities of memory cells).

Applicant's independent claims 1, 7 and 47, each recites, *inter alia*, a programmable logic integrated circuit (121) with a structure as defined in the specification (pages 7-24) including an arbiter (1510) coupled to the first and second ports, wherein the arbiter arbitrates access to the memory by the first port and the second port, wherein when the second port is accessing a subset of the first plurality of memory cells, the arbiter prevents the first port from accessing the first plurality of memory cells but allows the first port to access the second plurality of memory cells, and when the second port is accessing a subset of second plurality of memory cells, the arbiter allows the first port to access the first and second pluralities of memory cells. Applicant's independent claims 1, 7 and 47 each comprises a particular combination of element, which is nether taught or suggested by the prior art.

Accordingly, Applicant's claims are allowed for these reasons and for the reasons recited in the previous amendments and remarks.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Miller et al. (US PAT. 6,212,607 B1) discloses a dual-port memory device with a plurality of memory bank (201), semaphore logic (302), i.e., arbiter, arbitrates on a first received basis between access requests from left and right electronic devices (col. 4 lines 46-56), and left and right input/output control logic (305 and 306), which are located in a integrated circuit (200), wherein one of the memory bank granting exclusive access through individual ones of the at least two input/output ports to individual ones of the selected single-ported memory banks by receiving bank signal by the semaphore logic and the status registers (308 and 310). Miller et al. fails to teach a arbiter arbitrates access to the memory by the first and second ports, wherein when the second port is only accessing a subset of the first plurality of memory cells, the arbiter prevents the first port from accessing the first plurality of memory cells, but allows the first port to access the second plurality of memory cells, and when the second port is only accessing a subset of the second plurality of memory cells, the arbiter allows the first port to access both the first and second pluralities of memory cells.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H. Li whose telephone number is 571-272-4183. The examiner can normally be reached on Tues - Fri 9:00am - 6:30pm and alternate Monday..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Zhuo H. Li

Patent Examiner
February 22, 2006